Short Papers

Microwave Performances of n-p-n and p-n-p AlGaAs/GaAs Heterojunction Bipolar Transistors

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Abstract—**The performances of MOCVD-grown n-p-n and p-n-p AlGaAs/GaAs HBT's were compared at microwave frequencies to identify relative merits of each type of device. The f_t and f_{max} values of devices with 100-nm-thick bases were 22 and 40 GHz for n-p-n transistors and 19 and 25 GHz for p-n-p transistors, respectively. An accurate device model was developed using the measured S parameter data. The base resistance of the p-n-p transistors, as determined from the model, was about six times lower than identical size n-p-n devices. Output power and power-added-efficiencies of p-n-p devices were found to be half those obtained with n-p-n devices at 10 GHz.**

I. Introduction

Heterojunction bipolar transistors (HBT's) based on GaAs are gaining acceptance as high-power microwave amplifiers. Power densities as high as 2.5 W/mm of emitter periphery were demonstrated at 10 GHz [1]–[3] under CW conditions. Devices operating under pulsed conditions produced even higher power densities (5.4 W/mm) [3]. These power densities are a factor of 2 to 4 higher than GaAs FET's operating under similar conditions at this frequency. HBT's are also important for microwave applications because of their low phase noise characteristics. At 4 GHz, it was shown that HBT oscillator noise characteristics are similar to those of Si bipolar transistors and superior to those of GaAs FET's [4]. These performance advantages, coupled with the fact that HBT fabrication can be accomplished with optical lithography (minimum line width $\geqslant 2$ μm) for frequencies at least up to 40 GHz, continue to encourage the development of this device for microwave applications.

All high-performance (microwave and digital) HBT's to date have been of n-p-n type to take advantage of high electron mobility in III–V compound semiconductors. The n-p-n configuration is chosen by most designers because of the low series resistance that can be obtained in the emitter and collector regions. Also, the minority carrier mobility in the base is kept high. But these advantages are offset by the high resistance of the thin p-type base. It is important to keep the resistance of this layer low, especially for high-frequency operation. Low base resistance is usually obtained by heavily doping the base [5] or by the use of a narrower bandgap semiconductor as the base layer [6].

On the other hand, p-n-p transistors can have low base resistances because of higher mobility of electrons, but the emitter and collector resistances are increased. Although the mobility of holes in the collector is low, carriers are forced to travel at their saturated velocities through most of this layer, owing to the large electric fields that must be sustained for power generation. Therefore, the collector transit time delay is not much higher than in n-p-n counterparts. The only significant time delay encountered in p-n-p structures is the delay due to the diffusion of holes through the base layer. This is about a factor of 5 higher than in n-p-n structures of similar dimensions. Of course, p-n-p transistors can have narrower bases for a given base sheet resistance, which reduces this difference somewhat. Therefore, p-n-p HBT's can be considered for high performance microwave applications. More important, the availability of high-speed p-n-p transistors will enable the implementation of microwave complementary circuits, which has so far not been possible with GaAs.

The performance potential of p-n-p HBT's was analyzed recently [7], [8], and the performance potential was compared to that of n-p-n transistors [9]. The findings of these studies suggest that both types of devices will operate at similar speeds, provided that each is optimized in its own unique ways. Recently, microwave operation of p-n-p HBT's was demonstrated [10]. It was shown that the small-signal performance of p-n-p HBT's is comparable to that of n-p-n HBT's of similar size. This paper reports the results of a direct experimental comparison of the performances of n-p-n and p-n-p HBT's with identical structures. The aim of the study was to determine relative merits of each type of transistor in order to provide a base for future optimization studies. Both the small- and the large-signal properties were compared. A comprehensive device model was developed for both types of devices to aid in this comparison.

II. Design and Fabrication

The vertical structures of the transistors are shown in Table I. All epitaxial layers were grown in an atmospheric MOCVD system on an undoped semi-insulating substrate. The substrate surface was 2° off [100] toward the nearest [110]. Si and Zn were used as the dopants for n and p layers, respectively. A nominal growth rate of 10 Å/s was employed with group-V/group-III gas ratios of 15:1.

The emitter was made of $Al_{0.4}Ga_{0.6}As$ in both cases. The thicknesses of emitter, base, and collector were kept the same in both structures, but the doping concentrations in the base were different. An acceptor level of 1×10^{19} cm^{-3} was used for the base of n-p-n structures, whereas the donor concentration of the base for the p-n-p structure was 3×10^{18} cm^{-3}. These doping levels represent the highest levels that could be obtained at the typical growth temperature of 750°C. The subcollector layer was 1.0 μm thick in both cases. Thinner layers resulted in high series collector resistances in p-n-p devices, thereby limiting power performances. Much thicker layers were found to be proportionally more difficult to isolate, therefore the value chosen was a compromise between performance and fabrication ease. The performance of HBT's (especially p-n-p types) can be further improved by increasing the thickness of this layer.

No intentional spacer layers or bandgap grading was employed in these structures. It is, however, reasonable to assume that the

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TABLE I
VERTICAL STRUCTURE FOR n-p-n AND p-n-p HBT'S

npn			pnp		
Layer	Thick-ness (μm)	Doping (cm-3)	Layer	Thick-ness (μm)	Doping (cm-3)
n^+ - GaAs	0.2	3E18	p^+ - GaAs	0.2	1E19
n-$Al_{0.4}Ga_{0.6}As$	0.2	2E17	p-$Al_{0.4}Ga_{0.6}As$	0.2	2E17
p^+ - GaAs	0.1	1E19	n^+ - GaAs	0.1	3E18
n - GaAs	1.0	3E16	p - GaAs	1.0	3E16
n^+ - GaAs	1.0	3E18	p^+ - GaAs	1.0	3E18
SI Substrate	500	--	SI Substrate	500	--

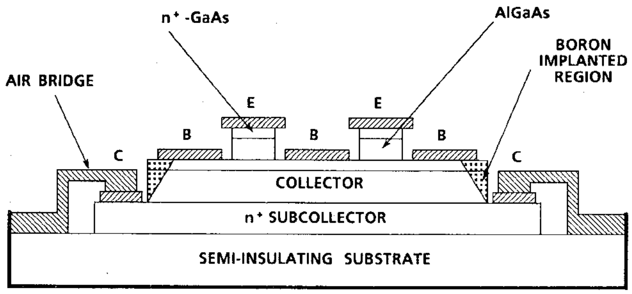


Fig. 1. The vertical structure of n-p-n and p-n-p HBT's.

heterointerface between the emitter and the base is exponentially graded over a distance of about 10 nm due to the temperature and growth rates employed in typical MOCVD runs. The structures shown in Table I yielded devices with base-collector breakdown voltages of about 20 V.

A self-aligned fabrication technique [1] was used to place the base contact as close to the emitter as possible. Fig. 1 is a cross-sectional drawing and Fig. 2 is a SEM picture of the completed device. Emitter and base finger widths were kept constant at 2 μm in the design of all devices studied here. The total emitter periphery ($2 \times$emitter length$+2\times$emitter width) was 60 μm. Two collector contacts were used as shown in Fig. 2 to minimize the series resistance at the device output port. The chip size was 0.4 mm$\times$0.3 mm$\times$0.1 mm. AuGe/Ni was used as the contact metal for all n-type layers, including the base layer of p-n-p devices. TiPtAu was used as the contact metal for p-type layers, excluding the subcollector of p-n-p devices. For this layer AuZn alloy was used. TiPtAu does not form an alloyed contact to p-type GaAs, but the doping levels used in these layers were high enough to yield acceptable contact properties. In the device model described below, TiPtAu contacts to p-type layers were characterized as Schottky contacts. Although AuZn-based alloys produced better contact properties, they were found unsuitable for thin layers from the viewpoint of reliability. However, since the subcollector layer is the lowest (nearest to the substrate) conductive layer in the HBT structure and is relatively thick (1 μm), AuZn-type contacts did not present a reliability problem for this layer. Mesa isolation was used to separate device active areas. All contact pads were fabricated on the surface of the SI GaAs substrate. Air bridges were used to connect device terminals to these pads as indicated in Fig. 1.

III. RESULTS AND DISCUSSION

Fig. 3 shows the dc characteristics of the devices fabricated. In both cases β values in excess of 50 could be obtained. Important differences between the characteristics of n-p-n and p-n-p transistors can be identified as an increased emitter/collector series resistance in p-n-p devices as evidenced by the slope of the linear portion of the $I-V$ curves; an increased offset voltage of 0.5 V in p-n-p devices, compared with 0.2 V observed with n-p-n; and a lower Early voltage with p-n-p transistors.

Small-signal characteristics of the devices were determined using the HP 8510 automatic network analyzer in the frequency range of 0.25 to 26.5 GHz. From these measurements, figure of merit numbers (f_t), common emitter current gain cutoff frequency, and maximum frequency of oscillation (f_{max}) were deter-

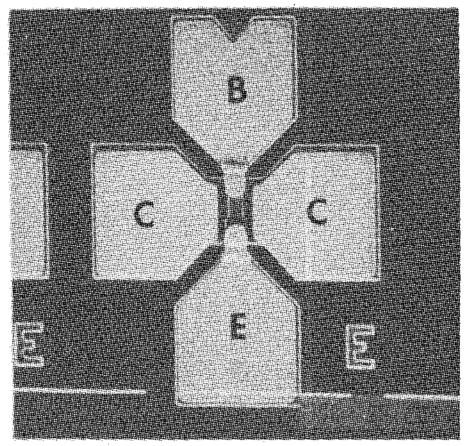
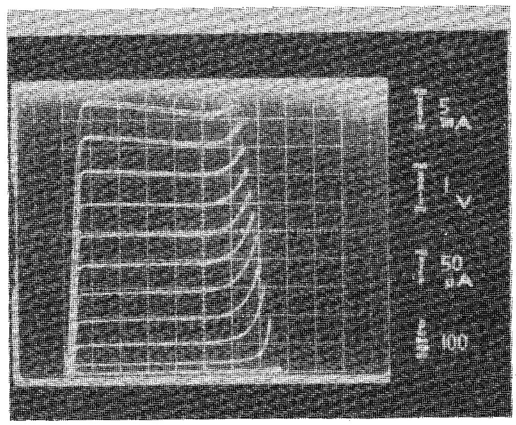
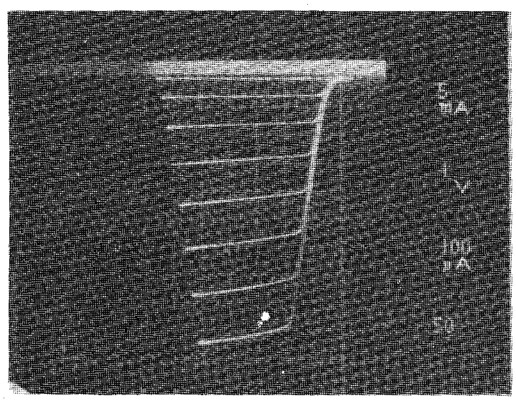


Fig. 2. SEM picture of the 60 μm emitter periphery device.

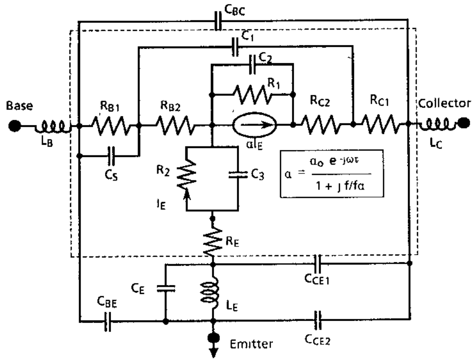


(a)



(b)

Fig. 3. dc characteristics: (a) n-p-n HBT. (b) p-n-p HBT.



Parameter	NPN	PNP	Parameter	NPN	PNP
f_T	22 GHz	19 GHz	C_s	1 34 PF	0
f_{max}	40 GHz	25 GHz	R_{C1}	1 Ω	7 4Ω
α_o	93	96	R_{C2}	4Ω	3 3Ω
τ	2 ps	4 ps	R_E	8 5Ω	7 0Ω
$f\alpha$	65 GHz	35 GHz	C_{BC}	012 PF	012 PF
C_1	06 PF	04 PF	C_{BE}	022 PF	022 PF
C_2	01 PF	1 PF	C_{CE1}	012 PF	012 PF
C_3	4 PF	3 PF	C_{CE2}	06 PF	08 PF
R_1	1E6 Ω	1E6 Ω	C_E	022 PF	03 PF
R_2	10Ω	6 8Ω	L_B	165 nH	26 nH
R_{B1}	17Ω	3 0Ω	L_E	032 nH	09 nH
R_{B2}	27 5Ω	4 4Ω	L_C	06 nH	134 nH

Fig. 4. The equivalent circuit model and parameter values for 60 μm emitter periphery n-p-n and p-n-p HBT's.

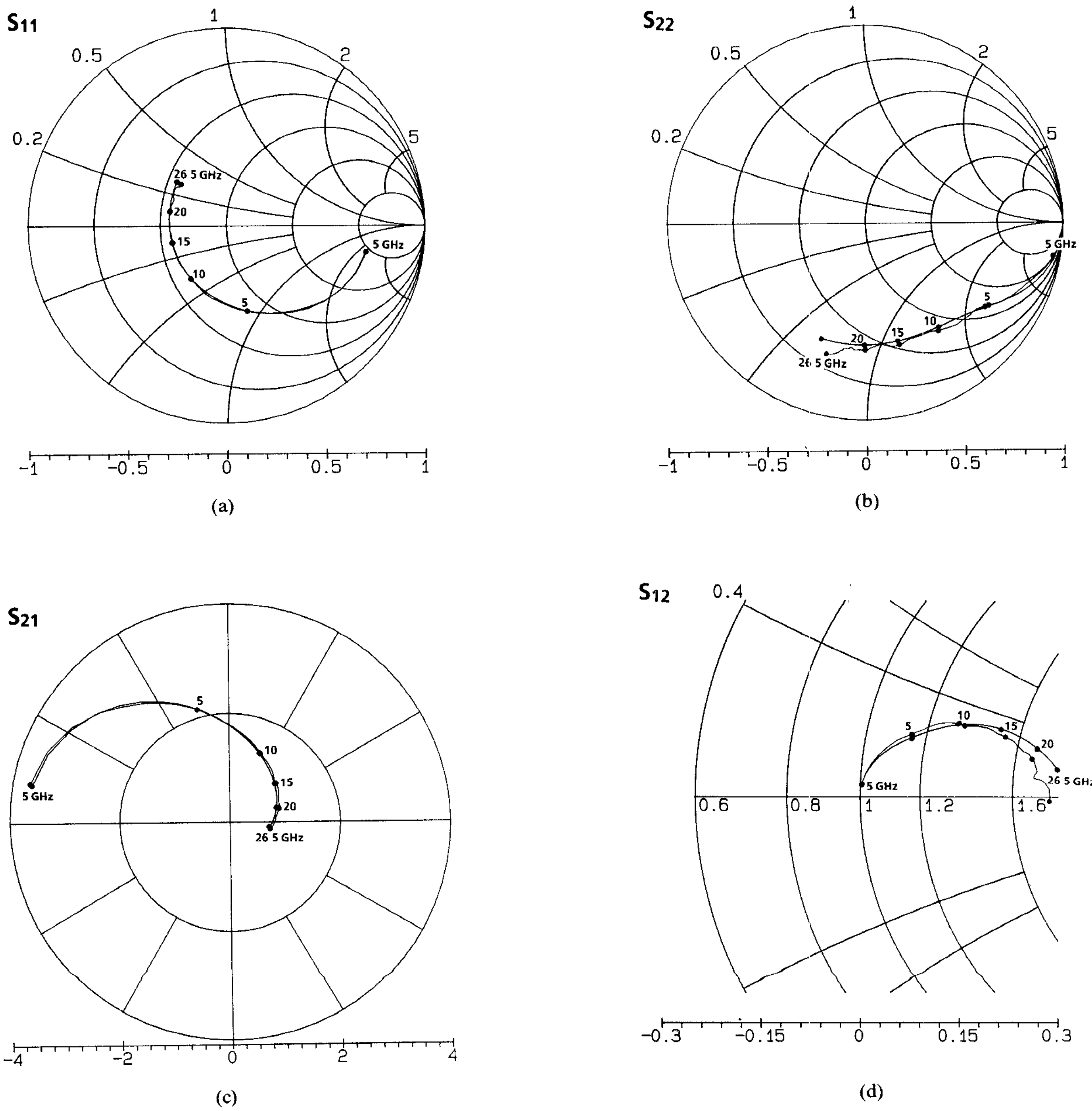


Fig. 5 Measured (ragged) and modeled S parameter data for a 60 μm emitter periphery n-p-n HBT

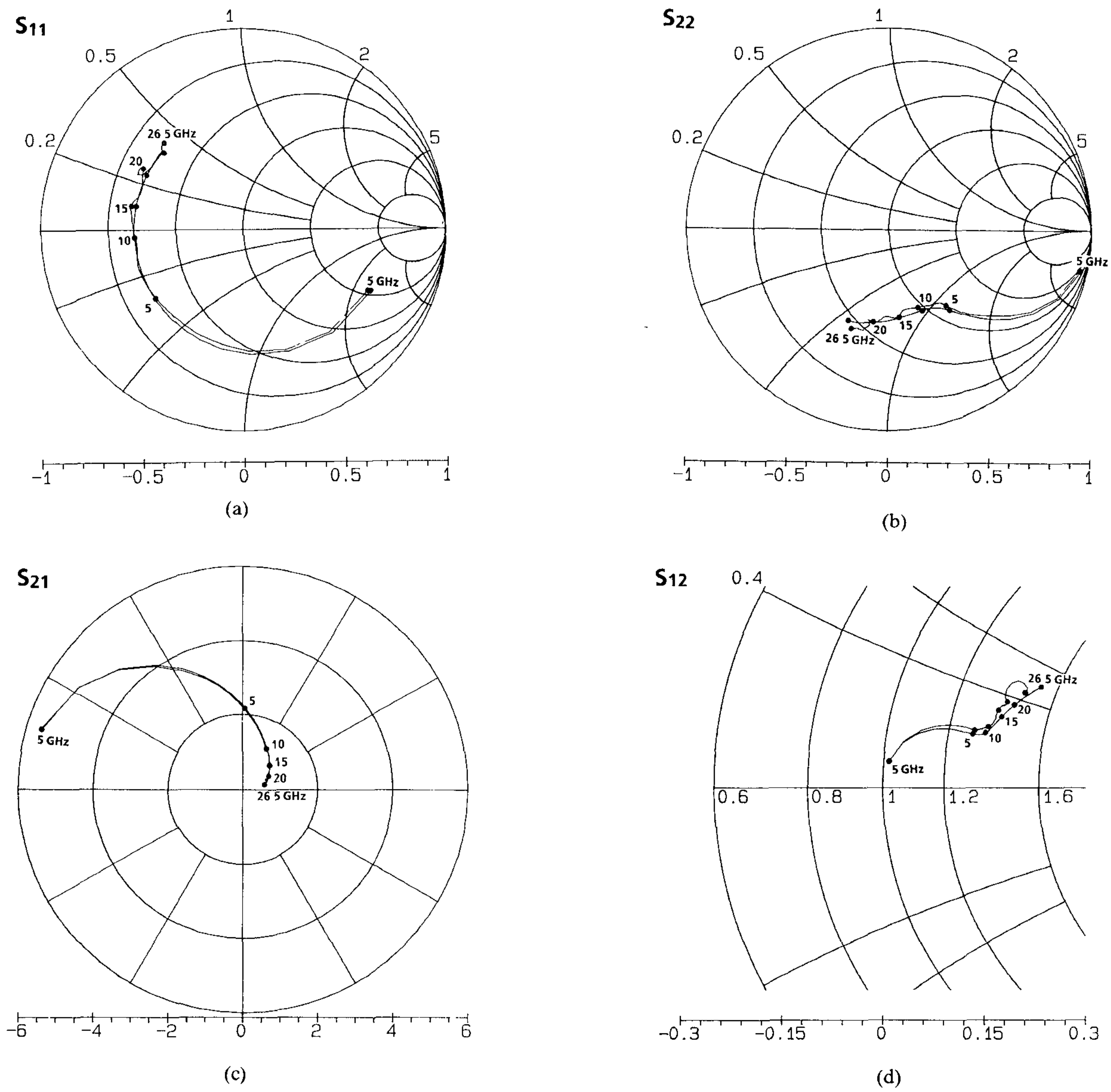


Fig. 6 Measured (ragged) modeled S parameter data for a 60 μm emitter periphery p-n-p HBT.

mined for each type of transistor. The values f_t and $f_{\max}$ were 22 and 40 GHz for n-p-n devices and 19 and 25 GHz for p-n-p devices, respectively. On the basis of these measurements we can state that the small-signal microwave performances of both types of devices are quite similar.

An equivalent circuit model was developed by computer fitting of the measured S parameter data to the circuit element values. Fig. 4 shows the equivalent circuit and the circuit element values for the 6 μm emitter periphery n-p-n and p-n-p transistors. The equivalent circuit was derived from the device design parameters and included the parasitic elements resulting from the air bridges and contact pads. The base contact resistance of the n-p-n transistors was modeled as a resistor in parallel with a capacitor. This was found to be necessary to obtain a better agreement at higher frequencies. The intrinsic device portion of the equivalent circuit is indicated by the area defined by the broken lines. Figs. 5 and 6 show the excellent agreement obtained between the measured and the modeled S parameters for both the n-p-n and the p-n-p transistors.

A closer examination of Fig. 4 indicates that the capacitive elements are almost the same for both devices, whereas some noteworthy differences exist in the resistive elements. The most important difference is in the base resistance. The p-n-p transistor has a base resistance ($R_{B1} + R_{B2}$) that is about a factor of 6 lower than that of its n-p-n counterpart. On the other hand, the collector series resistance is a factor of 7 higher in p-n-p transistors. Emitter resistors appear to be comparable in both cases. These observations are consistent with the lower mobility of p-type layers in each type of device.

Large-signal characteristics were determined by operating devices as amplifiers in common-base configuration at 10 GHz. Both CW and pulsed modes of operations were investigated. Table II lists the results obtained. It is seen that p-n-p HBT's produce approximately half the power density of n-p-n HBT's. The power-added efficiencies are also about half those of n-p-n devices. There are some similarities in the large-signal characteristics, however. The power densities in both devices almost double going from CW to pulsed modes of operation.

A comparison of the small- and large-signal results indicates that the speed of p-n-p devices is similar to that of n-p-n devices, but the power output and efficiencies are lower. This can be explained as a result of larger collector series resistances encoun-

TABLE II
LARGE-SIGNAL PERFORMANCES OF 60 μm EMITTER PERIPHERY n-p-n AND p-n-p HBT'S AT 10 GHz

Device Type	Operation Mode	Output Power (mW)	Power Density (W/mm)	Gain (dB)	Power Added Efficiency
npn	CW	120	2.0	6	40%
npn	Pulsed	300	5.0	8	50%
pnp	CW	70	1.15	4	21%
pnp	Pulsed	120	2.0	5	25%

tered in p-n-p devices. Since this resistor is on the output side of the device, it has a significant effect on the power performance. A reduction in this parasitic resistor is necessary for improving power output and can be accomplished by the use of thicker subcollector layers and lower resistivity ohmic contacts.

IV. CONCLUSIONS

Microwave performances of n-p-n and p-n-p AlGaAs/GaAs HBT's with 100-nm-thick bases were compared. Although the small-signal characteristics were found to be similar, the power output capability of p-n-p devices was about half that obtained from n-p-n devices. Further optimization of the p-n-p structure, especially the subcollector layer, will probably result in devices comparable in performance. The availability of high-performance n-p-n and p-n-p HBT's will make it possible to implement complementary microwave and high-speed digital circuits.

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GaAs Power MESFET Performance Sensitivity to Profile and Process Parameter Variations

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Abstract —**Large-signal performance sensitivities are calculated and compared for power GaAs MESFET's fabricated with uniform, ion-implanted, and lo–hi–lo conducting channel doping profiles. The large-signal sensitivities of the RF power and power-added efficiency are determined for the device designs as a function of variations in various process-dependent parameters. It is demonstrated that the channel doping profile design and breakdown voltage have the most significant influence upon large-signal RF performance.**

I. INTRODUCTION

The rapid development of the state of the art in monolithic microwave integrated circuits has intensified the need to develop sophisticated CAD tools for use in circuit and device design. There is a particular need for large-signal device models capable of describing the nonlinear characteristics of active devices at microwave frequencies. In order to obtain the maximum benefit from a device simulator, the device model should be capable of describing the performance of a device before fabrication. In this manner much time, effort, and expense would be saved since device optimization studies could be performed before the device were actually fabricated. This consideration indicates a physics-based model, and the need to simulate RF operation indicates an analytic approach. Most of the large-signal device models presented to date, however, are based upon equivalent circuit techniques and require that the device be fabricated and characterized before the equivalent circuit is established. Since device characterization is, at best, an inexact process [1], the accuracy of the equivalent circuit techniques is not well established.

A physics-based, analytic large-signal GaAs MESFET model suitable for RF applications has recently been reported [2]. In this paper this model is used to investigate the large-signal RF performance sensitivities of GaAs power MESFET's to various device design and process-dependent parameters. The RF performances of power FET's with uniform, ion-implanted, and lo–hi–lo (buried channel) doping profile designs are considered and compared.

II. DEVICE MODEL

The device model used in this work [2] is based upon efficient solutions to the basic semiconductor device equations. The model solves a simplified form of the device equations analytically in

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